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| EXAMINER |
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| WASSUM, LUKE S |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2177 | |

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/643,316 | BROOKLER ET AL. | |
| | Examiner | Art Unit | |
| | Luke S. Wassum | 2177 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Priority*

1. The Applicants' claim to domestic priority under 35 U.S.C. §119(e) to provisional patent application 60/149,855, filed 19 August 1999, is acknowledged.

2. Since the subject matter of the provisional application essentially encompasses that of the instant application, a priority date of 19 August 1999 is hereby established.

### *Drawings*

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "320-322" have been used to designate records in both the manufacturers and categories tables. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 320-322. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

*Embodiment of the Invention*

5. The claimed invention is a method of using bit vector indexes in order to increase the efficiency of database querying.

*Claim Objections*

6. Claims 14, 35, 42, 48, 56 and 63 are objected to because of the following informalities:

There appears to be typographical errors in claims 14, 35 and 56. The examiner believes that the Applicants intended these claims to depend from claims 13, 34 and 55 respectively, and not claims 9, 30 and 51.

There appears to be a typographical error in claim 48. The examiner believes that the Applicants intended this claim to depend from claim 47, and not claim 50.

There appears to be typographical errors in claims 42 and 63, wherein the claimed limitation is determining whether the bit vector representations are 'effected'. The correct word is 'affected'.

Appropriate correction is required.

*Claim Rejections - 35 USC § 112*

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-15, 19, 22-28, 40, 43-57 and 61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claims 1, 22 and 43 are vague, unclear, and/or indefinite. In these claims, the term 'value' is used ambiguously.

In the preamble and steps 1, 2 and 3, the term 'value' refers to the association of a specific data value (e.g., 1, 'Apex', 'Monitor') and a specific data field (e.g., Manufacturer ID, Manufacturer, Category). For example, a 'value' could be 'Manufacturer ACME'.

In the fourth step, however, the term 'value' refers to the '1' or '0' entered in the bit position to represent the presence or absence of the specific data value cited above.

In the fifth step, the value refers to the contents of the field of the data record under consideration.

Furthermore, in the fifth step, the claimed step is that the 'bit position' is synchronized to reflect updates to the value. However, it is the *contents* of the bit position that is synchronized, and it must reflect updates to the *contents of the field of the data record under consideration*, not to the value. The value (as defined in the preamble and in steps 1, 2 and 3) cannot change, since the bit vector itself represents this specific value.

10. Claims 2-15, 23-36 and 44-57, incorporating the above cited deficiencies, are therefore also rendered indefinite.

11. Claims 19, 40 and 61 are vague, unclear, and/or indefinite. In these claims, it is stated that performing a logical "AND" will result in a single result representing whether any of the at least one data records contains a combination of the at least first and second values. However, the result of such a logical "AND" operation will represent whether any of the records contain the first value and

any of the records contain the second value; the values need not occur in the same record for a logical "AND" to return a '1'.

For example, if record number 1 contains value1, and record number 2 contains value2, a bitwise "AND" operation (01 & 10) will correctly result in a 00, indicating that there are no records that contain both value1 and value2. However, a *logical* "AND" operation (01 && 10) will result in a 1, indicating that both values were non-zero. Note that the values (value1 and value2) need not be in the same record for the operation to return a positive result.

12. Claims 8, 24 and 50 recite the limitation "the encoded bit vector" in line 3. There is insufficient antecedent basis for this limitation in the claim.

13. Claims 11, 32 and 53 recite the limitation "the data structure" in line 2. There is insufficient antecedent basis for this limitation in the claim.

14. Claims 14, 35 and 56 recite the limitation "the bit-level operation" in line 2. There is insufficient antecedent basis for this limitation in the claim.

15. Claim 48 recites the limitation "the representation" in line 2. There is insufficient antecedent basis for this limitation in the claim.

*Claim Rejections - 35 USC § 102*

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. Claims 16-18, 37-39 and 58-60 are rejected under 35 U.S.C. 102(b) as being anticipated by **O'Neil et al.** [1] ("Improved Query Performance with Variant Indexes").

18. Regarding claims 16, 37 and 58, **O'Neil et al.** [1] teaches a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values, comprising:

a) creating a first bit vector representation for a first value, the first bit vector representation identifying use of the first value in the at least one data record (see the disclosure of the creation of bitmap indexes in section 2.1.1 Bitmap Indexes, page 39);

b) creating a second bit vector representation for a second value, the second bit vector representation identifying use of the second value in the at least one data record (see the disclosure of the creation of bitmap indexes in section 2.1.1 Bitmap Indexes, page 39); and

c) performing a bit-level operation on the first and second bit vector representations (see disclosure of the database query performance of Boolean operations, including "AND" and "OR" operations, on bitmap indexes, section 2.1.2, pages 39-40).

19. Regarding claims 17, 18, 38, 39, 59 and 60, **O'Neil et al.** [1] teaches a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values wherein the bit-level operation is a bit-wise "AND" returning a bit corresponding to each of the at least one data record identifying

whether a combination of the first and second values exist in the at least one data record (see disclosure of the database query performance of Boolean operations, including "AND" and "OR" operations, on bitmap indexes, section 2.1.2, pages 39-40).

*Claim Rejections - 35 USC § 103*

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

22. Claims 1-4, 11, 12, 22-25, 32, 33, 43-46, 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over **O'Neil et al.** [1] ("Improved Query Performance with Variant Indexes") in view of **Depledge et al.** (U.S. Patent 5,884,307).

23. Regarding claims 1, 22 and 43, **O'Neil et al.** [1] teaches a method, computer-readable medium and computer-executable process for indexing occurrences of a value in at least one data record using a bit vector representation, comprising:

a) associating a bit vector representation with a value (see section 2.1.1 Bitmap Indexes, page 39; the claimed value is anticipated by property P in the second paragraph of col. 2);

b) associating a bit position of the bit vector representation to the at least one record (see section 2.1.1 Bitmap Indexes, page 39, specifically col. 2, second paragraph, lines 1-4);

c) determining whether the value exists in the at least one data record (see section 2.1.1 Bitmap Indexes, page 39, specifically col. 2, second paragraph, lines 1-4); and

d) assigning a value to the bit position in the bit vector representation based on the outcome of the determining step (see section 2.1.1 Bitmap Indexes, page 39, specifically col. 2, second paragraph, lines 1-4).

**O'Neil et al.** [1] does not explicitly teach a method, computer-readable medium and computer-executable process including the step of synchronizing the bit position with the value to reflect any updates to the value.

**Depledge et al.**, however, teaches a method for updating a segmented bitmapped index (analogous to the claimed bit vector index) to reflect a change made to data upon which the segmented index is based (see Abstract; see also col. 2, line 65 through col. 3, line 32).

It would have been obvious to one of ordinary skill in the art to provide for the synchronization of the claimed bit vector with the data upon which the index is based, since for the

bitmapped indexes to remain valid, they must be updated whenever a change is made to the data upon which they are based (see col. 2, lines 25-37).

24. Regarding claims 2-4, 23-25 and 44-46, **O'Neil et al.** [1] additionally teaches a method, computer-readable medium and computer-executable process substantially as claimed, including the fact that the bit vector representation comprises a sequence of bits (see **O'Neil et al.** [1] page 39, col. 2, first sentence of the second paragraph), further comprising encoding the bit vector representation by determining whether a frequency of a binary digit is less than the number of bits used to store a number, and storing as the encoded bit vector representation at least one position of the binary digit in the bit vector representation (see disclosure that when the disk space required to hold a bitmap column index is comparable to the disk space required for the RID-list index, the representation is changed from a bitmap to a RID list, a rowed being analogous to the claimed position of the bit, page 39, last paragraph of section 2.1.1 Bitmap Indexes).

25. Regarding claims 11, 32 and 53, **O'Neil et al.** [1] additionally teaches a method, computer-readable medium and computer-executable process wherein the data structure is a record in a database (see disclosure of bitmap creation for 'the n rows of a table T', analogous to the claimed records in a database, page 39, col. 1, last paragraph).

26. Regarding claims 12, 33 and 54, **O'Neil et al.** [1] additionally teaches a method, computer-readable medium and computer-executable process further comprising examining the bit vector representation to determine whether the data record contains the value (see discussion of the bitmap index performance in section 2.1.2, pages 39-40).

27. Claims 5-10, 13-15, 26-31, 34-36, 47-52 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over **O'Neil et al.** [1] ("Improved Query Performance with Variant Indexes") in view of **Depledge et al.** (U.S. Patent 5,884,307) as applied to claims 1, 22 and 43 above, and further in view of **O'Neil et al.** [2] ("Multi-Table Joins Through Bitmapped Join Indices").

28. Regarding claims 5-7, 26-28 and 47-49, **O'Neil et al.** [1] and **Depledge et al.** teach a method, computer-readable medium and computer-executable process substantially as claimed, including the fact that the bit vector representation comprises a sequence of bits (see **O'Neil et al.** [1] page 39, col. 2, first sentence of the second paragraph).

Neither **O'Neil et al.** [1] nor **Depledge et al.** explicitly teaches a method, computer-readable medium and computer-executable process further comprising encoding the bit vector representation by determining whether the size of a region of like binary digits is twice number of bits used to store a number, and storing as the encoded bit vector representation a representation of the region.

**O'Neil et al.** [2], however, teaches a method, computer-readable medium and computer-executable process further comprising encoding the bit vector representation by determining whether the size of a region of like binary digits is twice number of bits used to store a number, and storing as the encoded bit vector representation a representation of the region (see the disclosure regarding run-length encoding, page 9, last sentence of the last paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to change the manner of storage as claimed, since this would save in data storage, as disclosed in the last paragraph of page 9.

29. Regarding claims 8-10, 29-31 and 50-52, **O'Neil et al.** [1] and **Depledge et al.** teach a method, computer-readable medium and computer-executable process substantially as claimed.

Neither **O'Neil et al.** [1] nor **Depledge et al.** explicitly teaches a method, computer-readable medium and computer-executable process wherein the bit vector representation is encoded and compressed using a compression technique.

**O'Neil et al.** [2], however, teaches a method, computer-readable medium and computer-executable process wherein the bit vector representation is encoded and compressed using a compression technique (see the disclosure regarding bitmap compression, including run-length encoding, page 9, bottom of the last paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to change the manner of storage as claimed, since this would save in data storage, as disclosed in the last paragraph of page 9.

30. Regarding claims 13-15, 34-36 and 55-57, **O'Neil et al.** [1] additionally teaches a method, computer-readable medium and computer-executable process wherein plural bit vector representations exist each representing a discrete value, and further comprising determining whether

the data record contains more than one of the values by performing a bit-level operation that includes "OR" and "AND" on the corresponding bit vector representations (see disclosure of the database query performance of Boolean operations, including "AND" and "OR" operations, on bitmap indexes, section 2.1.2, pages 39-40).

31. Claims 19, 40 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over **O'Neil et al.** [1] ("Improved Query Performance with Variant Indexes") as applied to claims 16-18, 37-39 and 58-60 above, and further in view of **Schildt** ("C: The Complete Reference").

32. Regarding claims 19, 40 and 61, **O'Neil et al.** [1] teaches a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values substantially as claimed.

**O'Neil et al.** [1] does not explicitly teach a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record wherein the "AND" operation is a logical "AND" returning a single result representing whether any of the at least one data records contain a combination of the first and second values.

**Schildt**, however, teaches the use of the logical "AND" operator to determine whether or not all of the expressions are non-zero (see pages 47-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the logical "AND" operator, since this would allow a user to determine whether or not the first and second bit vector representations were both non-zero.

33. Claims 20, 21, 41, 42, 62 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over **O'Neil et al.** [1] ("Improved Query Performance with Variant Indexes") as applied to claims 16-18, 37-39 and 58-60 above, and further in view of **Depledge et al.** (U.S. Patent 5,884,307).

34. Regarding claims 20, 21, 41, 42, 62 and 63, **O'Neil et al.** [1] teaches a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values substantially as claimed.

**O'Neil et al.** [1] does not explicitly teach a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values further comprising updating at least one data record, determining whether the updating has affected any of the bit vector representations, and if so, updating the affected bit vector representations.

**Depledge et al.**, however, teaches a method for updating a segmented bitmapped index (analogous to the claimed bit vector index) to reflect a change made to data upon which the segmented index is based (see Abstract; see also col. 2, line 65 through col. 3, line 32).

It would have been obvious to one of ordinary skill in the art to provide for the synchronization of the claimed bit vector with the data upon which the index is based, since for the bitmapped indexes to remain valid, they must be updated whenever a change is made to the data upon which they are based (see col. 2, lines 25-37).

*Conclusion*

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

**Millett et al.** (U.S. Patent 4,817,036) teaches a system for database bit vector indexing and information retrieval.

**French et al.** (U.S. Patent 5,649,181) teaches a system for bit vector indexing of a database.

**Chadha et al.** (U.S. Patent 5,706,495) teaches a system for encoded vector indexing of a database.

**Fulton et al.** (U.S. Patent 5,799,184) teaches a system that uses bitmasks to index a database.

**Chen et al.** (U.S. Patent 5,852,821) teaches a system for indexing a database through the use of bit vectors.

**Depledge et al.** (U.S. Patent 5,899,988) teaches a system of bitmapped indexing of a database.

**Ozbutun et al.** (U.S. Patent 5,963,935) teaches a method of combining bitmap indexes and compression when a memory use limit is reached.

**Vagnozzi** (U.S. Patent 6,070,164) teaches a database that uses fine and coarse sliced bit vector indexing.

**Egan et al.** (U.S. Patent 6,405,187) teaches a system that uses encoded vector indexing in a database.

**Babb** ("Implementing a Relational Database by Means of Specialized Hardware") teaches hardware using bit vectoring to speed execution of queries.

**Schneider et al.** ("A Performance Evaluation of Four Parallel Join Algorithms in a Shared Nothing Multiprocessor Environment") teaches the use or bit-vectoring techniques in parallel join algorithms.

**Chaudhuri et al.** ("An Overview of Data Warehousing and OLAP Technology") teaches the use of bit map indices in a data warehouse.

**Perrizo et al.** ("A Query Processing Method for Data Warehouses Which Contain Multimedia") teaches the background of bitmap indexes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke S. Wassum whose telephone number is 703-305-5706. The examiner can normally be reached on Monday-Friday 8:30-5:30, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Breene can be reached on 703-305-9790. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

In addition, INFORMAL or DRAFT communications may be faxed directly to the examiner at 703-746-5658.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Luke S. Wassum
Art Unit 2177

lsw
March 7, 2003

JEAN R. HOMERE
PRIMARY EXAMINER